**Remarks**

Regarding the objections to the Drawings in sections 1 and 3 of the Office Action, we respectfully submit that the objections are without merit and should be withdrawn. The Applicant respectfully submits that the Figures sufficiently show all of the features of the claims. We remind the examiner that the figures and specification are directed to a person skilled in the art, who is familiar with STS frames. There are 810 bytes in an STS frame, and to show each byte, with each pointer offset would needlessly clutter the figure. To do so would not only fail to improve the understanding to a person skilled in the art, but would make actually obscure the important the portions that would be most helpful to a person skilled in the art. We respectfully submit that a person skilled in the art, in conjunction with the specification, would readily understand that the pointer offset 522, 492, and indeed the pointer itself is implicit in the figure. Accordingly we respectfully submit that the Figures are fully compliant with rule 1.83.

With respect to section 2 of the Official Action regarding the objections to the Drawings, we have amended the specification to include reference number 58, rendering the objection to the drawings in Section 2 of the Office Action moot.

With respect to section 4 of the Office Action, we thank the examiner for noticing this error. The specification has been corrected.

With respect to sections 5-15 of the Office Action, we have amended the claims appropriately.

With respect to section 16 of the Office Action, we have corrected an error (the missing "where") on page 9 of the specification, which we believe may have been the source of the examiner's assumptions. However, the double negative is clear in this claim, and while similar to claim 7, claim 9 is not wholly redundant with it. For example, claim 7 does not state IF and ONLY IF, and therefore, claim 9 is not necessarily implied by claim 7.

With respect to the anticipation rejection in section of 18 of the Office Action, we traverse the rejection as follows.

Regarding claim 1, 11 and 19:

First, we point out that Baydar teaches a system whose purpose is different than that of the claimed invention. The cited passages do not teach a "method for managing latency" as alleged in the rejection. Rather, Badyar teaches a method for transferring data streams (e.g. STM, VT/TU) from one timing domain to another (via a pointer processor). Baydar uses control information and memories (buffers/FIFOs) for the purpose of retiming incoming data streams to the system clock (leveraging the pointer processing methods described in the SONET/SDH standards).

Furthermore, and because of this difference, Baydar does not in fact teach

> "adjusting a pointer for the low-order sources **based on the provisioning bit** such that the high-order and low-order outputs are synchronized."

as claimed. The cited section does refer to a pointer interpreter and a JSYNCH signal, but it does not teach adjusting the pointer based on a provisioning bit in order to synchronize the high-order and low-order outputs. The JSYNCH signal is used for timing purposes, in order to find the start of the payload of the high-order signal as the delay through the pointer processor memory is not fixed (predetermined). However, this is not the same as, and the cited sections do not teach, synchronizing the high-order(HO) and low-order(LO) signals as claimed.

Furthermore, the cited sections do not teach adjusting a pointer "**based on the provisioning bit**". To the extent Baydar uses a provisioning bit, it uses such a provisioning bit for a different purpose than that of the claimed invention, and therefore does not teach adjusting the pointer based on the provisioning bit (to synch the HO and LO outputs) as claimed. To the extent Baydar uses a provisioning bit, it uses such a provisioning bit to determine what signals contain LO, in order to know when to process the LO signals (e.g. the V1/V2 pointer bytes). However, it does not adjust the pointer based on the provisioning bit, and certainly does not adjust the pointer based on the provisioning bit in order to synchronize the HO and LO signals.

Accordingly, we respectfully submit that the rejection to claims 1, 11 and 19 is deficient and should be withdrawn.

Regarding claim 2 and 12 (and 3, 13 and 20), we respectfully submit that the cited passage does note teach the claimed subject matter. For example, as Baydar's incoming pointer is not known, Baydar (or at least the cited passage) does not teach a pointer adjustment by a predetermined delay (e.g. claim 2) or a predetermined number of time slots (e.g., claim 3). For example, see Baydar, Col 8, line 1-17 -- which we submit describes how the effective delay (latency) through the elastic store IS NOT fixed and predetermined and that it floats based on fill level.

We respectfully submit that the rejection to the remaining claims are overcome at least for the reasons given. Furthermore, with respect to the obviousness rejections, we respectfully submit that a person skilled in the art would not modify the teachings of Baydar to achieve the claimed subject matter as Baydar teaches a different system, for a different purpose than the claimed subject matter, and in addition because of the differences set out above

Accordingly, we respectfully submit the rejections have been traversed. Withdrawal of the rejections and allowance of the application is hereby requested.

No fee is believed due for this submission. However, Applicant authorizes the Commissioner to debit any required fee from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP. The Commissioner is further authorized to debit any additional amount required, and to credit any overpayment to the above-noted deposit account.

Respectfully submitted,

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